Evaluating FLEX 6000 Performance

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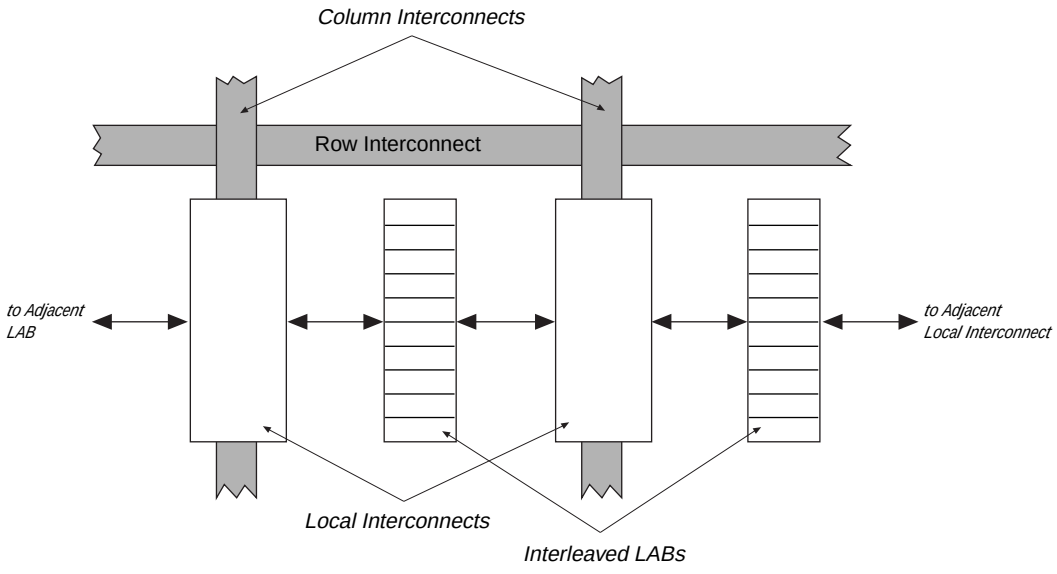
The Altera® FLEX™ 6000 family offers leading-edge performance at a price that is competitive with gate arrays. FLEX 6000 devices are based on the OptiFLEX™ architecture, which combines interleaved logic array blocks (LABs), an optimized I/O structure, and an advanced bond pad pitch to achieve twice the performance at about half the price of FPGAs. While an ASIC may still be the only solution for the highest-performance requirements, this technical brief evaluates how the high performance and low cost of the FLEX 6000 device family makes it a viable alternative for many gate array designs.

OptiFLEX Architecture

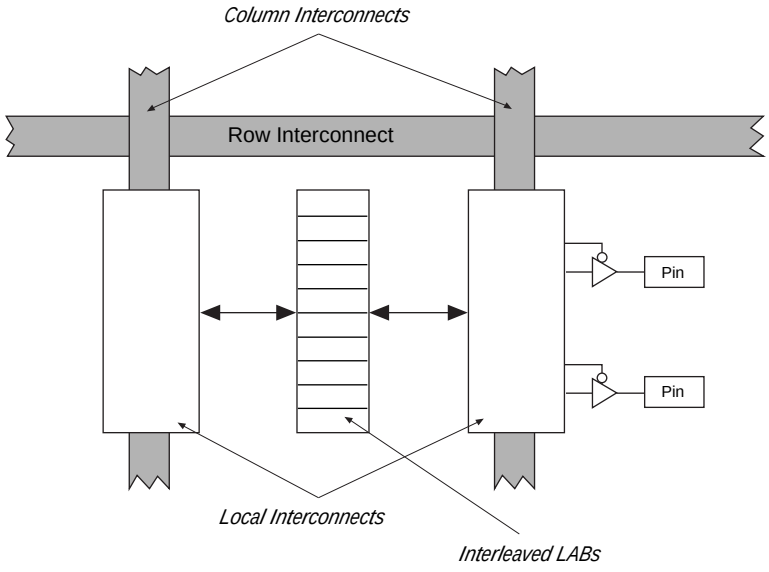
The OptiFLEX architecture combines the speed and predictability of Altera's continuous FastTrack™ Interconnect with interleaved LABs and FastFLEX™ I/O features. The interleaved LAB structure enables logic elements (LEs) to communicate within the same LAB and with neighboring LABs via local interconnect. Each LE can drive two local interconnects and can communicate directly with 19 LEs through high-speed local resources, which minimizes row and column delays and increases performance and efficiency. See Figure 1.

Figure 1. Interleaved LAB Feature of the FLEX 6000 Architecture



The FastFLEX I/O feature enables an LE to drive an I/O pin through local interconnect for fast clock-to-output timing and I/O register performance. With this feature, the OptiFLEX architecture can support PCI timing specifications with minimal die size. See Figure 2.

Figure 2. FastFLEX I/O Feature of the FLEX 6000 Architecture



Price & Performance Comparison

Table 1 compares the price and performance of the EPF6016 device with the Xilinx XC5210 and XC4013E devices.

Table 1. Comparison of EPF6016 vs. XC5210 & XC4013E Devices *Note (1)*

Benchmark	EPF6016		XC5210			XC4013E	
	-2	-3	-3	-4	-5	-2	-3
16-bit loadable counter (MHz)	135	99	65	59	50	76	65
16-bit accumulator (MHz)	135	99	–	–	–	76	65
24-bit accumulator (MHz)	99	72	50	45	39	–	–
16-to-1 multiplexer (ns)	5.5	7.0	9	11	13	–	–
100-unit list price (208-pin QFP)	$32.50	$22.95	$81.30	$68.70	$57.25	$224.00	$166.00

Note:
(1) Sources: Altera *FLEX 6000 Programmable Logic Device Family Data Sheet* and price list for third quarter 1997; and Xilinx XC5200 and XC4000 Field Programmable Gate Array Data Sheets and June 1997 pricing.

Table 1 shows that the EPF6016 device costs less and performs faster than the XC5210 and XC4013E devices. These advantages are possible because the OptiFLEX architecture is designed to produce maximum performance in the smallest possible die size. Because the XC5200 and XC4000E devices are based on coefficient segmented architectures, they require a larger die size to increase performance, which results in higher costs.

With the low-cost structure of FLEX 6000 devices, designers can prototype their designs with programmable logic devices (PLDs) and stay with PLDs for volume production without having to migrate their designs to an ASIC. To achieve the highest performance and utilization with FLEX 6000 devices, designers must optimize their design for the FLEX 6000 architecture. Retargeting designs that have been optimized for a gate array will not produce optimal results.

Optimization through Design Methodology

The performance and utilization of FLEX 6000 devices also depends on the design methodology used. Table 2 compares the performance and utilization results of the EPF6016 device and a 0.5-µ gate array. It shows the typical results of a 16-bit counter using two different HDL design methodologies: inferred and instantiated.

Table 2. 16-Bit Counter Results Using Two Different Methodologies

Device	Design Methodology			
	Inferred		Instantiated	
EPF6016 Device	65 LEs	58 MHz	16 LEs	135 MHz
0.5-µ Gate Array	342 Gates	104 MHz	337 Gates	106 MHz

The first design methodology infers a 16-bit loadable counter with synchronous clear function in Verilog HDL. The second methodology instantiates the same counter function that has been optimized for the FLEX 6000 architecture. Instantiating the function results in marginal utilization and performance improvements for the gate array. In contrast, the EPF6016 device uses 75% fewer LEs and achieves 133% higher performance.

This comparison is not meant to show that FLEX 6000 devices are faster than an ASIC; instead, it shows the impact that design methodology can have on a PLD architecture. In this example, the EPF6016 device is faster than the gate array because a 16-bit counter is more ideally suited for its FLEX 6000 architecture. With some up-front design planning, designers can achieve large gains in FLEX 6000 device utilization and performance, effectively eliminating the need to migrate to gate arrays for volume production.

The documents listed below provide more detailed information. Part numbers are in parentheses.

- *FLEX 6000 Programmable Logic Device Family Data Sheet (A-DS-F6000-02)*
- *AN 87: Configuring FLEX 6000 Devices (A-AN-087-01)*

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